REMARKS

Reconsideration of the application, in view of the following amendments and remarks is respectfully requested.

The Examiner objects to the drawing stating that Figure 1 should be designated by a legend such as –prior art— because only that which is old is illustrated. A corrected drawing is enclosed herewith in which this figure has been labeled Prior Art.

The Examiner rejects Claims 20 and 30 under 35 U.S.C. 112, first paragraph, as failing to comply with the written descripton requirement. The Examiner states that the claims contains subject matter which is not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors at the time the application was filed, had possession of the claimed invention. The Examiner states that paragraph 34 of the specification describes the capacitors as being discrete but the claims state the capacitors are integrated in the semiconductor device. The Examiner states that no other parts of the specification describe these capacitors as being integrated in the specification as evidenced by all figures which all have the capacitors as discrete components, therefore, the specification does not reasonably convey how these capacitors are integrated in the semiconductor device.

This rejection is respectfully traversed. Actually, paragraph 34 says the opposite of what the Examiner states. Paragraph 34 states, in part:

> "One illustrative embodiment of capacitor integration according to the present invention is depicted in Fig. 4. In Fig. 4, one embodiment 400 of the present invention has capacitors 222, in addition to transistors 224, integrated into semiconductor device 201. Only capacitor 206 and system 214 utilize discrete components. As with transistors 224, the integrated capacitors 222

may be combined with transistors 224 – all within device 210." (emphasis added)

Furthermore, paragraph [0026] recites, in pertinent part, starting at line 5;

> "This target voltage is set sufficiently low enough to enable integration of some or all componentry within array 220 into a commercially viable semiconductor process."

Paragraph [0033] also recites:

> "In instances where available semiconductor processes are capable of forming the required capacitors in an efficient manner, integration of all capacitors may be provided - ...".

Furthermore, Fig. 4 clearly shows all of the capacitors 222 within the integrated circuit which is shown in the dotted lines in Fig. 4. Accordingly, Applicants request that this rejection be withdrawn as incorrect.

The Examiner rejects Claims 1-19, 20-29, and 30-35 under 35 U.S.C. 103(a) as being unpatentable over Applicant's admitted prior art in view of Bowers et al. The Examiner states that with respect to Claim 1, Applicant's Figure 1, which is prior art, disclose a load, a primary component , and a secondary array in parallel to the primary component. The Examiner states that Applicant's Figure 1 does not disclose a reduction system, however, Bowers et al discloses a driver connected to a resonant structure thus making it analogous art since it is in the same field of endeavor. The Examiner states that Bowers et al teaches a reduction system of element 118 driver circuit to a resonant circuit in Figure 7a and Column 6, lines 24-38. The Examiner concludes that it would be obvious to one of ordinary skill in the art at the time of the applicant's invention, to add the reduction system as taught by Bowers et al to a

resonant structure in order to better match the impedance from the driver circuit to the resonant circuit.

We cannot not agree. First of all, Applicants are not impedance matching, the Examiner's statements to the contrary notwithstanding. Secondly, there's no element 118 in Figure 7a of Bowers et al, and Applicants assume the Examiner meant element 18 and are responding herewith on that basis. As clearly shown in Fig. 6, which is the same circuit in block form as Fig. 7a, element 18 is a coupling capacitor which is meant to block the DC component only. It is used in the conjunction with the circuit 16 to match the impedance between the supply driver 14 and the output resonant circuit 12. It has nothing to do with the reduction in voltage of the present invention. Bowers is not related to the trimming of the resonant frequency or reducing the voltage, the Examiner's statement to the contrary notwithstanding and therefore does not, in combination with the admitted prior art render the present invention obvious.

The claims have been amended in order to more clearly recite that the present invention forms a voltage divider between the reduction system and the primary component in order to reduce the operational voltage at the node to a target value. It is this reduction that allows for the integration of all of or portions of the trimming circuit 222, 224 into an integrated circuit, where this is desired. As well known to those skilled in the art, this results in a dramatic reduction in the price and size of the unit. The ability to integrate the circuit is provided by the reduction system because the voltages that would otherwise be present across the capacitor elements are far too high to be accommodated even by the newest semiconductor integrated circuit technology.

Accordingly, Applicants believe that the application, as previously amended, is in condition for allowance, and such action is respectfully requested.

Respectfully submitted by,
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